## ABSTRACT OF THE DISCLOSURE

A branch prediction apparatus having a primary predictor and a secondary predictor that selectively overrides the primary predictor based on the type of branch instruction decoded. A branch target address cache in the primary branch predictor speculatively predicts a branch target address and direction based on an instruction cache fetch address prior to decoding the instruction, and the processor branches to the speculative target address if the speculative direction is predicted taken. Later in the pipeline, decode logic decodes the instruction and determines the branch instruction type, such as whether the branch instruction is a conditional branch, a return instruction, a program counter-relative type branch, an indirect branch, etc. Depending upon the branch type, if the primary and secondary predictions do not match, the processor branches based on the secondary prediction to override the branch taken based on the primary prediction.